PP4

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/475,262	12/30/1999	BEN D. ROBERTS	042390.P6809	6144

7590 09/08/2003

DARREN J MILLIKEN
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
7TH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025

EXAMINER	
CRAIG, DWIN M	
ART UNIT	**PAPER NUMBER**
2123	5

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/475,262	ROBERTS, BEN D.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☒ Claim(s) ~~4~~ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-63 have been presented for reconsideration in light of Applicant's amended claims.

Response to Arguments

2. Applicant's arguments filed on 6-20-2003 have been fully considered. Examiners response is as follows:

2.1 Regarding Applicant's response to the rejections of Claims 1, 28, 29, 33 and 60:

Applicant has argued that;

> "To establish a prima facie case of obviousness ... the prior art reference (or references when combined) must teach or suggest all the claim limitations." MPEP 2143 The Applicant respectfully submits that each of the Applicant's independent claims 1, 28, 29, 33 and 60 are patentable over the combined teachings of Nakamura, Muddu and Dansky at least because the combined teachings of Nakumura, Muddu and Dansky fail to disclose, teach or suggest "reducing a string to a pi model, the pi model having a pair of cross capacitors" or "a pair of cross capacitors associated with a pi model, the pi model reduced from a string". The Applicant supports the insufficiency of the Examiner's theory of rejection by way of the following discussion of each of the Nakumura, Muddu and Dansky references and their application to the claim elements at issue.
>
> Nakamura is an irrelevant prior art reference with respect to "reducing a string to a pi model, the pi model having a pair of cross capacitors" or "a pair of cross capacitors associated with a pi model, the pi model reduced from a string". The string to which the Applicant's claims refer is "a lumped element model of a trace". See, Applicant's specification page 9, lines 20-21. By contrast, the string of Nakamura represents *"the surface* of. . . a semiconductor element. See, Nakamura, Col. 7, lines 23-36. Thus, whereas the Applicant's string is related to circuit modeling (e.g., including resistances, capacitances, etc.), Nakamura's string is related to the simulation of a manufactured semiconductor wafer's surface topography (e.g., so as to involve specific processing steps and materials such as "vacuum vapor deposition" and "Ti"). Therefore Nakamura has absolutely no relevance to the Applicant's use of the term "string"

The Examiner asserts that the *Nakamura* reference does disclose using a string model **(Figure 3).** The Examiner asserts that the *Nakamura* reference supports the notion

that a string model is useful in modeling circuit elements in the fabrication of a circuit design.

In response to applicant's argument that *Nakamura* reference is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the *Nakamura* reference is directed towards electronic circuit simulation. The string model disclosed would be very useful in determining the parasitic electronic elements in an integrated circuit where the pathways for possible influence from nearby circuit traces could be complex.

Examiner asserts that grouping lumped elements and using a pi-model are also well known in the art and that is why, when looked at in its entirety, the combination of the *Nakamura, Muddu and Dansky* references disclose all of the Applicant's claimed limitations. The Applicant has not provided a factual reason for the *Nakamura, Muddu and Dansky* references to not be combined and has instead provided a *piecemeal* argument listing the deficiencies of each reference without addressing the combined limitations disclosed by the combination of these references. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The Muddu reference is directed to efficiently simulating the effects of interconnect line delay between gates rather than simulating the effects of coupled noise between interconnect lines. As such, although Muddu teaches the use of a pi model for circuit modeling, Muddu limits itself only to representing a single interconnect tree with a pi model without regard for any cross capacitance that may exist; and, likewise, Muddu does not disclose, teach, suggest or refer to anything that relates to cross capacitance or noise.
That Muddu is directed solely to interconnect line delay rather than coupled noise between interconnect lines is notorious in various instances. Most notably, Col. 1, lines 18 - 40 and Fig. 1 of Muddu only refer to or show interconnection lines between gates and do not refer to or show capacitive coupling between interconnection lines. By contrast, page 2, line 11 through page 4, line 7 and Fig. 1 A of the Applicant's specification clearly refers to a pair of interconnect lines and the capacitive coupling that exists between them so as to introduce unwanted noise upon an interconnect line. Moreover, the pi modeling techniques ("accurate" and "open-endedlheuristic") taught by Muddu are clearly devoted only to the analysis of a single interconnect tree without reference to capacitive coupling between other interconnect trees (e.g., see, Muddu Col. 5, lines 41 - 44: "[i]n the O'BrienISavarino (accurate RC) fl model, the interconnect tree load is approximated by an RC fl model with a resistance and capacitance equaling the total interconnect resistance (Rtot) and capacitance (Ctoc), respectively. . . "; and see, Muddu Col. 6, lines 16 - 21: " . . . [t]he open-ended RC Il model approximates the entire interconnect tree 104 by an equivalent open-ended RC line whose resistance (Rtot) and capacitance (Ctot) 104d are equal to the total interconnect resistance and capacitance, as shown in FIG. 5(a)"). Lastly, Muddu appears to make no reference to coupling between neighboring interconnect lines, cross capacitance, noise and the like.
As such, Muddu simply does not disclose teach or suggest "reducing a string to a pi model, the pi model having a pair of cross capacitors" or "a pair of cross capacitors associated with a pi model, the pi model reduced from a string".

The Examiner asserts that the *Muddu* reference relies on the *Nakamura* reference for a string model for simulating a group of lumped circuit elements. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Capacitive Coupling) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Unlike Muddu, the Dansky reference is directed to the effects of crosscoupled noise. The only discussion of a model as taught by Dansky appears at Col. 7, lines 9 - 60. Note that the model of Dansky does not include a pair of cross capacitors and only includes a single cross capacitor model element (See, Dansky, Col. 7, line 16: "2. Mutual capacitance between the two nets (C12 mf)"). Moreover, even if Dansky employs such a model for each and every path/segment of a interconnect net (See, Dansky, Col. 6 line 21 through Col. 7, line 9) it is clear that no reduction process is described. Better said, if Dansky reduces the entire net to the model described at Col. 7, lines 9 - 60; then, Dansky does not teach a model having a "pair of cross capacitors". Or, if Dansky models an entire net by forming the model of Dansky for each path/segment of a net; then, Dansky does not teach a reduction process.

Either way, Dansky cannot be said to disclose, teach or suggest: "reducing a string to a pi model, the pi model having a pair of cross capacitors" or "a pair of cross capacitors associated with a pi model, the pi model reduced from a string".

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The Examiner has found Applicant's arguments to be unpersuasive and upholds the earlier 35 U.S.C. 103 rejections of Claims 1, 28, 29, 33 and 60.

Claim Objections

3. **Claim 17** is objected to because of the following informalities: in line 3 at the end of the sentence there is the phrase "resistors **is** series" this phrase should be changed to "resistors **in** series". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-3, 5-13, 15-20, 22-35, 37-45, 47-52 and 54-63** are rejected under 35 U.S.C. as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view of **Dannsky et al. U.S. Patent 6,028,989.**

4.1 As regards independent **Claims 1, 18, 28, 29, 33, 50 and 60** the *Nakamura* reference discloses, a machine readable storage medium with at least one processor **(Figure 35 Item 6, Col. 7 Lines 39-50)**, and a string model **(Figures 3, 5, 6, 9, 22A, 22B, 23, 24, 25, 26, 27, 28, 30A, 30B, 30C, 34).**

However, the *Nakamura* reference does not expressly disclose modeling a trace lumped elements, cross capacitors, a pi model and applied noise voltage.

The *Muddu* reference discloses modeling a trace **(Figure 1),** a pi model **(Figures 8b, 8c).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because

(motivation to combine) when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

The *Nakamura* reference does not expressly disclose lumped elements, cross capacitors and applied noise voltage.

The *Dannsky et al.* reference discloses lumped elements **(Col. 7 Lines 9-67, Col. 8 Lines 1-6)** cross capacitors **(Col. 7 Line 16),** and applied noise voltage **(Col. 1 Lines 15-18, Lines 63-67, Col. 2 Lines 1-17).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

4.2 As regards the limitation disclosed in independent **Claim 28** regarding an apparatus, the *Nakamura* reference discloses **(Figure 35).**

4.3 As regards **Claims 2, 3, 5, 19, 20, 22, 23, 34, 35, 37, 51, 52 and 54** the *Nakamura* does not expressly disclose reducing the number of capacitors and resistors in the model and the O'Brien/Savarino method.

The *Muddu* reference discloses reducing the number of capacitors and resistors in the model and the O'Brien/Savarino method, **(Figure 4, Col. 5 Lines 35-67, Col. 6 Lines 1-67, Col. 7 Lines 1-2).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

4.4 As regards **Claims 6, 38 and 55** the *Nakamura* reference does not expressly disclose a "pi" model.

The *Muddu* reference discloses a "pi" model **(Figure 8b and 8c).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

4.5 As regards **Claims 7, 32, 39, 56 and 63** the *Nakamura* reference does not expressly disclose a voltage ramp.

The *Muddu* reference discloses a voltage ramp **(Figure 2b).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models

that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

4.6 As regards **Claims 8, 24 and 40** the *Nakamura* reference does not expressly disclose a ramp time and a driving transistor.

The *Muddu* reference discloses a ramp time and a driving transistor **(Figures 1, 2a, 2b, 3, 4, 5a, 5b, 6a, 6b, 7a, 7b, 8a, 8b, 8c, 8d and 8e, Col. 3 Lines 44-67, Col. 4 Lines 1-67, Col. 5 Lines 1-67, Col. 6 Lines 1-67, Col. 7 Lines 1-2).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

4.7 As regards **Claims 9 and 41** the *Nakamura* reference does disclose a string model, however it does not expressly disclose a pi model.

The *Muddu* reference discloses a pi model **(Figures 8b, 8c).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

4.8 As regards **Claims 10 and 42** the *Nakamura* reference does not expressly disclose a linear source.

The *Muddu* reference discloses a linear source model **(Figures 8a, 8c, Col. 8 Lines 8-14).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

4.9 As regards **Claims 11, 12, 43, 44 and 57** the *Nakamura* reference does not expressly disclose a victim node of the pi model.

The *Dansky et al.* reference discloses a victim node of the pi model **(Col. 1 Lines 24-26, Col. 3 Lines 15-16, Col. 3 Lines 40-48).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

4.10 As regards **Claims 13, 26, 27, 58 and 59** the *Nakamura* reference does not expressly disclose a second noise voltage to the pi model.

The *Dansky et al.* reference discloses a second noise voltage applied to the pi model **(Col. 3 Lines 40-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

4.11 As regards **Claims 15, 16 and 25** the *Nakamura* reference does not expressly disclose calculating the peak noise.

The *Dansky et al.* reference discloses calculating peak noise **(Col. 7 Lines 60-67, Col. 8 Lines 1-6).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

4.12 As regards **Claims 17 and 49** the *Nakamura* reference does not expressly disclose resistors in series and capacitors in parallel reduced into a pi-model.

The *Muddu* reference discloses resistors in series **(Figure 5a, 5b, Col. 6 Lines 15-25)** and capacitors in parallel **(Figures 8b, 8c).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models

that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

4.13 As regards **Claims 30 and 61** the *Nakmura* reference does not expressly disclose discrete samples.

The *Mudda* reference discloses discrete load capacitances **(Col. 4 Lines 14-22).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Muddu* reference because *(motivation to combine)* when designing with sub-micron design rules for integrated circuit design accurate models for interconnect delay of logic gates are required for functional models that reflect the true functioning on the silicon substrate before expensive fabrication is performed, ***(Muddu, Col. 1 Lines 15-67, Col. 2 Lines 1-50).***

4.14 As regards **Claims 31, 45, 47, 48 and 62** the *Nakamura* reference does not expressly disclose applied noise voltage.

The *Dannsky et al.* reference discloses applied noise voltage **(Col. 1 Lines 15-18, Lines 63-67, Col. 2 Lines 1-17).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Dannsky et al.* reference because *(motivation to combine)* it is important to calculate in an efficient manner the voltage noise characteristics of an integrated circuit design ***(Dannsky et al. Col. 1 Lines 55-67, Col. 2 Lines 1-33).***

5. **Claims 4, 21, 36 and 53** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view

of **Dannsky et al. U.S. Patent 6,028,989** and in further view of **"Modeling the Driving-Point Characteristics of Resistive Interconnect for Accurate Delay Estimation", Peter R. O'Brien and Thomas L. Savarino, IEEE 1989** hereafter referred as the **O'Brien and Savarino** reference.

5.1 As regards independent **Claims 1, 18, 33, 50** see the rejection in paragraph **3.1.**

5.2 As regards dependent **Claims 2, 3, 19, 20, 34, 35, 51 and 52** see the rejection in paragraph **4.3.**

5.3 As regards **Claims 4, 21, 36, 53** the *Nakamura* reference does not expressly disclose the Elmore influence reduction method.

The *O'Brien and Savarino* reference discloses the Elmore influence reduction method **(pages 513-514).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *O'Brien and Savarino* reference because *(motivation to combine)* the methods disclosed in the *O'Brien and Savarino* reference provides greater accuracy in determining the voltage transfer ration between gates in an integrated circuit, ***(Abstact, Page 512 "Modeling the Driving-Point Characteristics of Resistive Interconnect for Accurate Delay Estimation", Peter R. O'Brien and Thomas L. Savarino, IEEE 1989).***

6. **Claims 14 and 46** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nakamura U.S. Patent 6,192,330** in view of **Muddu U.S. Patent 6,314,546** and in further view of **Dannsky et al. U.S. Patent 6,028,989** and in further view of **Arsenault et al. U.S. Patent 6,396,256.**

6.1 As regards independent **Claims 1 and 33** see the rejection in paragraph **4.1.**

6.2 As regards dependent **Claims 13 and 45** see the rejection in paragraph **4.10 and 4.14** respecively.

6.3 As regards **Claims 14 and 46** the *Nakamura* reference does not expressly disclose voltage ramps having their ramp times in phase.

The *Arsenault et al.* reference discloses voltage ramps having their ramp times in phase **(Figures 2 and 3, Col. 1 Lines 45-55, Col. 2 Lines 48-63).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Nakamura* reference with the *Arsenault et al.* reference because *(motivation to combine)* the *Arsenault et al.* reference discloses a method of detecting defects in a design before manufacturing and therefore remove the requirement to have to redesign a product after the initial investment in manufacturing has been made, ***(Arsenault et al. Col. 1 Lines 34-45).***

Conclusion

7. After reconsideration the Examiner has found applicant's arguments to be unpersuasive. Claims 1-63 are rejected. Claim 17 is objected to.

7.1 THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
September 5, 2003